Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application:

Claims 21-24 (Cancelled).

25. (New) A circuit implementation of a biological neuron, the circuit comprising:

(a) a plurality of neuron circuits comprising:

a neuron cell membrane circuit;

a learning circuit coupled to said neuron cell membrane circuit; and

a dendrite circuit coupled to said neuron cell membrane circuit; and

(b) a synapse circuit coupled to each of said plurality of neuron circuits to provide a path through which said plurality of neuron circuits communicate and to modify synaptic conductance, said synapse circuit coupled to each of said neuron circuits through the corresponding dendrite circuit.

26. (New) The circuit of Claim 25 wherein said synapse circuit comprises:

a storage element having a first terminal coupled to a first terminal of said synapse circuit and a second terminal coupled to a second terminal of said synapse circuit;

a non-NMDA receptor channel circuit having a first terminal coupled to the first terminal of said synapse circuit and a second terminal coupled to the second terminal of said synapse circuit; and

an NMDA receptor channel circuit having a first terminal coupled to the first terminal of said synapse circuit and a second terminal coupled to the second terminal of said synapse circuit.

27. (New) The circuit of Claim 26 wherein said storage element comprises:

an amplifier; and

a capacitor having a first terminal coupled to an output terminal of said amplifier and a second terminal coupled to a first reference potential.

28. (New) The circuit of Claim 27 wherein said synapse circuit is coupled to said cell membrane circuit of said neuron circuit through said dendrite circuit.

29. (New) The circuit according to claim 25, wherein the neuron circuit emulates calcium influx via the NMDA receptor channel circuit.

30. (New) The circuit according to claim 25, wherein the cell membrane circuit includes four parallel legs such that three of the four legs include a voltage source representing reverse potentials of ions and one of the four legs includes a lumped capacitance.

31. (New) The circuit according to claim 25, further including further voltage sources representing reverse potentials of ions comprising one or more ligand-dependent potassium ion currents of a delayed rectifier current, an inward rectifier current, an A-current (IKA), and a calcium dependent potassium current (IAHP).

32. (New) The circuit according to claim 25, wherein the synapse circuit includes a threshold detection circuit, a signal conversion and formatting circuit coupled to the threshold detection circuit, and a storage device coupled to the signal conversion and formatting circuit.

33. (New) The circuit according to claim 25, further including a calcium concentration measurement circuit coupled to the NMDA receptor channel circuit.

34. (New) The circuit according to claim 33, wherein the calcium concentration measurement circuit includes

means for receiving signals from the non-NMDA receptor channel circuit and the NMDA receptor channel circuit;

means for measuring a net charge over time flowing through the NMDA receptor channel circuit; and

a temporary storage and buffer circuit for accumulating the net charge over time flowing through the NMDA receptor channel circuit.

35. (New) The circuit of Claim 34, wherein said temporary storage and buffer circuit comprises a capacitor and wherein said current is accumulated in said capacitor such that said capacitor has a voltage which is proportional to the charge.

36. (New) The circuit of Claim 35 further comprising:

means for scaling the current flowing through the NMDA receptor channel circuit; and

means for accumulating a scaled copy of the NMDA current onto the capacitor such that the voltage on the capacitor represents a concentration of Ca^{2+} ions.

37. (New) The circuit of Claim 33 further comprising a threshold detection circuit, said threshold detection circuit comprising:

first means for providing a plurality of reference voltages; and

second means, coupled to said first means, for receiving an input voltage and for comparing the input voltage to each of said plurality of reference voltages and for providing an output voltage in response to said comparison.

38. (New) A circuit to emulate a biological neuron, comprising:

a plurality of circuit means for providing neuron circuits; and

a synapse circuit coupled to the plurality of circuit means to provide a path through which said plurality of circuit means communicate and to modify synaptic conductance, said synapse circuit coupled to said circuit means through the corresponding dendrite circuit.

39. (New) The circuit according to claim 38, wherein the synapse circuit includes a storage element, a non-NMDA channel receptor circuit, and a NMDA channel receptor circuit coupled in parallel.

40. (New) The circuit according to claim 38, wherein the synapse circuit includes a threshold detection circuit, a signal conversion and formatting circuit and a storage device coupled in series.

41. (New) The circuit according to claim 38, wherein the plurality of circuit means emulate calcium influx via the NMDA receptor channel circuit.

42. (New) The circuit according to claim 38, further including a calcium concentration measurement circuit coupled to the NMDA receptor channel circuit.

43. (New) A method of implementing a biological neuron in a circuit, comprising:

implementing a plurality of neurons in a circuit each including

a neuron cell membrane circuit;

a learning circuit coupled to said neuron cell membrane circuit; and

a dendrite circuit coupled to said neuron cell membrane circuit; and

implementing a synapse in a circuit coupled to each of said plurality of neuron circuits to provide a path through which said plurality of neuron circuits communicate and to modify synaptic conductance, said synapse circuit coupled to each of said neuron circuits through the corresponding dendrite circuit.

44. (New) The method of Claim 43 further including implementing the synapse circuit to include:

a storage element having a first terminal coupled to a first terminal of said synapse circuit and a second terminal coupled to a second terminal of said synapse circuit;

a non-NMDA receptor channel circuit having a first terminal coupled to the first terminal of said synapse circuit and a second terminal coupled to the second terminal of said synapse circuit; and

an NMDA receptor channel circuit having a first terminal coupled to the first terminal of said synapse circuit and a second terminal coupled to the second terminal of said synapse circuit.

45. (New) The method of Claim 44 further including implementing the storage element to include:

an amplifier; and

a capacitor having a first terminal coupled to an output terminal of said amplifier and a second terminal coupled to a first reference potential.

46. (New) The method of Claim 45 further including implanting the synapse circuit to be coupled to said cell membrane circuit of said neuron circuit through said dendrite circuit.

47. (New) The method according to claim 46, further including implementing the synapse circuit to include a threshold detection circuit, a signal conversion and formatting circuit coupled to the threshold detection circuit, and a storage device coupled to the signal conversion and formatting circuit.

48. (New) The method according to claim 46, further including implementing a calcium concentration measurement circuit coupled to the NMDA receptor channel circuit.

49. (New) The method according to claim 48, further including implementing the calcium concentration measurement circuit to includes

means for receiving signals from the non-NMDA receptor channel circuit and the NMDA receptor channel circuit;

means for measuring a net charge over time flowing through the NMDA receptor channel circuit; and

a temporary storage and buffer circuit for accumulating the net charge over time flowing through the NMDA receptor channel circuit.

50. (New) The method of Claim 49, further including implementing the temporary storage and buffer circuit to include a capacitor and wherein said current is accumulated in said capacitor such that said capacitor has a voltage which is proportional to the charge.

51. (New) The method of Claim 50 further including implementing

a means for scaling the current flowing through the NMDA receptor channel circuit; and

means for accumulating a scaled copy of the NMDA current onto the capacitor such that

the voltage on the capacitor represents a concentration of Ca^{2+} ions.

52. (New) The method of Claim 47 further including implementing a threshold detection circuit, said threshold detection circuit comprising:

first means for providing a plurality of reference voltages; and

second means, coupled to said first means, for receiving an input voltage and for comparing the input voltage to each of said plurality of reference voltages and for providing an output voltage in response to said comparison.